What Is Claimed Is:

1. An apparatus for supporting a microprocessor development system, which comprises:

means for communicating data and control signals with respect to a target board through a multiplicity of ports, and providing a RAM address, a specific function register (SFR) address and data; and

means for receiving the RAM address, the SFR address and the data through the ports, providing the received data to the target board and controlling data to be input to the communicating means.

2. The apparatus as recited in claim 1, wherein the receiving means includes:

a port data decoder for receiving the RAM address or the SFR address and for decoding the received RAM or SFR addresses to develop a first output signal and a plurality of decoded output signals;

a controller for receiving the RAM or SFR data and the first output signal;

a first set of multiplexers for selectively transmitting the RAM or SFR data to the target board through a selected port in response to output signal from the controller and the port data decoder.

3. The apparatus as recited in claim 1, wherein the multiplexer includes:

a three-phase buffer responsive to the controller for outputting a plurality of buffer signals corresponding to the selected ones of the plurality of decoded output signals and the RAM or SFR data; and

a second multiplexer for selecting one of the plurality of data from the target board in response to the port data decoder.

4. The apparatus as recited in claim 1, wherein the communicating means further includes a multiplicity of I/O ports for inputting/outputting general data and address therethrough.

5. The apparatus as recited in claim 4, wherein each of the multiplicity of the I/O ports includes:

a first multiplexer having first and second input terminals and being controlled by an address selection signal, wherein the first multiplexer receives the RAM address or the SFR address at the first input terminal and a program code low address at the second input terminal; and

a second multiplexer having first and second input terminals and being controlled by an MDS test signal, wherein the second multiplexer receives an output of the first multiplexer at the first input terminal and the RAM data or the SFR data at the second input terminal.

6. An apparatus for supporting a microprocessor development system, which comprises:

a target board having a plurality of fictional circuits;

a MUC chip for receiving a program codes and providing the program to the target board;

a plurality of storage blocks connected to an interface through which a programmer check up results of the program;

a decoder for receiving and decoding address signals to access one of the storage blocks;

a multiplexor for selecting one of data transmitted through a plurality of pins in the target board in response to the coded output signals from the decoder.

7. The apparatus as recited in claim 6, wherein the MUC chip has an I/O port including:

a first multiplexer having first and second input terminals and being controlled by an address selection signal, wherein the first multiplexer receives the RAM address or the SFR address at the first input terminal and a program code low address at the second input terminal; and

a second multiplexer having first and second input terminals and being controlled by an MDS test signal, wherein the second multiplexer receives an

output of the first multiplexer at the first input terminal and the RAM data or the SFR data at the second input terminal.

8. The apparatus as recited in claim 6, wherein the storage blocks are RAM or register blocks.

9. The apparatus as recited in claim 8, wherein the decoder includes:

a port data decoder for receiving the RAM or register address and for decoding the received RAM or register addresses to develop a first output signal and the decoded output signals;

a controller for receiving the RAM or register data and the first output signal;

a first set of multiplexers for selectively transmitting the RAM or register data to the target board through a selected port in response to output signal from the controller and the port data decoder.